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Article

Research on Modulation Strategy and Power Balancing Method Optimization of Cascaded H-Bridge Inverter

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Abstract: Compared to symmetric cascaded H-bridge inverters (CHB), hybrid cascaded inverter technology can generate more voltage levels with fewer inverter units. In traditional inverter modulation strategies, hybrid cascaded inverters produce high-quality voltage output. However, due to power imbalance among cascaded units, the uneven power distribution accelerates unit degradation, thereby affecting the overall lifespan of the inverter. To address these issues, this paper proposes a novel modulation strategy. The low-voltage units undergo carrier reconstruction, while the high-voltage units employ modulation wave reconstruction, achieving power balancing across all units. The low-voltage units exhibit improved power-balancing response speed compared to traditional methods. Simulation results validate the effectiveness of the proposed approach.

Keywords: hybrid cascaded inverter; carrier reconstruction; modulation wave reconstruction; power balancing

1. Introduction

Cascaded H-bridge inverters (CHBIs) play a crucial role in renewable energy systems due to their simple structure, ease of installation and maintenance, wide power regulation range, and high output voltage stability. To reduce harmonic content during DC-to-AC conversion, inverters require more voltage levels to synthesize the AC waveform. Traditional CHBIs necessitate cascading additional devices to increase the number of levels, which significantly raises manufacturing costs.

Since the groundbreaking work by the Manjrekar team in 1996, hybrid cascaded H-bridge inverters with asymmetric DC-side voltages have emerged as a key development direction in multilevel inverter technology [1]. This architecture optimizes the number of cascaded units, enhancing output voltage levels while improving waveform quality. Modulation strategies, as core control elements of multilevel inverters, have evolved alongside system performance improvements. Fundamental solutions include the Specific Harmonic Elimination PWM (SHEPWM) and staircase modulation based on low-frequency modulation. In power balancing research, existing approaches differ in their methods and trade-offs. One study proposed a dynamic power-balancing algorithm through switch drive signal reconstruction, enhancing low-voltage unit balancing speed but requiring high computational power [2]. Another approach simplified implementation by using carrier reconstruction, though this reduced dynamic response speed [3]. Additionally, a state-machine-based method was introduced to improve IPD-PWM modulation [4]. Notably, while hybrid multi-carrier PWM techniques show advantages in harmonic suppression for seven-level CHB inverters at low modulation indices, their applicability to five-level topologies remains limited. This paper focuses on a nine-level hybrid inverter topology, proposing a carrier reconstruction mechanism based on degree-of-freedom analysis. A dynamic power-balancing model is innovatively established, revealing its time-domain response characteristics. By introducing voltage constraints for high-voltage units, autonomous power balancing is achieved across the full modulation range,

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shortening the low-voltage unit balancing cycle while ensuring system stability. Simulations and experiments validate the strategy's effectiveness through metrics such as THD, dynamic response, and voltage fluctuation, providing new theoretical and practical solutions for resolving the trade-off between power balancing and harmonic suppression in multilevel inverters.

2. Symmetric CHB Inverter Multi-Carrier PWM Modulation Technology

2.1. Symmetric CHB Inverter Topology

The symmetric CHB inverter topology is shown in Figure 1. Each cascaded unit is powered by an independent DC source, with DC-side voltages $U_{dc1} = U_{dc2} = U_{dc3} = E$. The AC-side output voltages of each unit are u_{H1}、u_{H2}、u_{H3}, and the phase voltage u_{AN} satisfies $u_{AN} = u_{H1} + u_{H2} + u_{H3}$ [5].

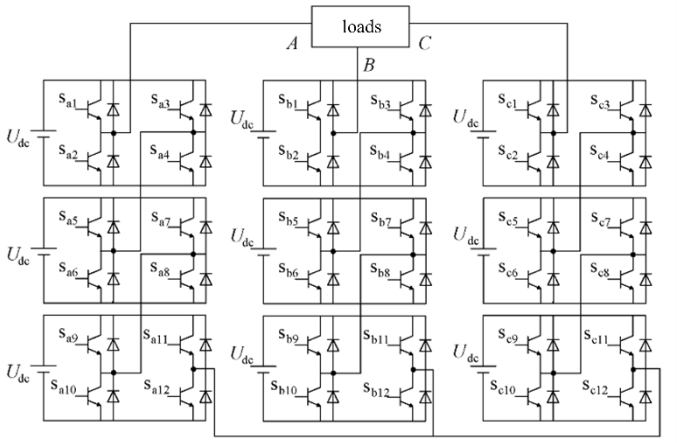


Figure 1. Three-phase cascaded H-bridge seven-level inverter circuit topology.

This circuit employs a multi-unit single-phase H-bridge cascaded structure for voltage synthesis. When switch pairs S11/S21, S12/S22, and S13/S23 are triggered simultaneously, the forward voltages of all H-bridge units superimpose to form a 3E phase voltage u_{AN}. Conversely, triggering S31/S41, S32/S42, and S33/S43 generates a -3E reverse voltage. By precisely scheduling switching combinations, the topology produces seven discrete voltage levels: ±3E, ±2E, ±E, and zero [6]. This architecture is defined as a seven-level cascaded H-bridge converter due to its programmable output states.

2.2. Selective Harmonic Elimination Pulse Width Modulation Technique

In the 1980s, American scholars Hasmukh S. Parekh and Richard G. Hoft pioneered a revolutionary waveform control methodology for inverter output voltage based on Fourier theory, establishing the Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) technique. This approach decomposes the inverter's output waveform into Fourier series while leveraging half-wave and quarter-wave symmetries to simplify harmonic equations. By formulating nonlinear equation systems constrained to eliminate N-order harmonics, the technique achieves precise switching angle solutions that nullify targeted harmonic amplitudes, enabling high-fidelity sinusoidal waveform reconstruction with minimal switching events.

Compared with SPWM and SVPWM, SHEPWM demonstrates three distinctive advantages in multilevel inverter applications: First, its harmonic elimination algorithm reduces Total Harmonic Distortion (THD) below 3% — a benchmark performance. Second, it achieves DC-link voltage utilization up to 1.15 times theoretical maximum, representing 15-20% improvement over conventional methods. Third, its fundamental frequency switching mode decreases device losses by 30-40%, making it particularly advantageous

for industrial frequency converters and renewable energy grid integration. However, the critical challenge lies in real-time solving of transcendental equations — traditional Newton-Raphson methods exhibit computational instability and deficient global convergence when modulation indices fall below 0.6 or approach unity, while intelligent optimization algorithms struggle to meet microsecond-level real-time control demands. This mathematical conundrum significantly hinders its application in dynamic operational scenarios.

2.3. Analysis of Traditional Multi-Carrier Schemes

Modulation schemes critically influence the output characteristics and power quality of CHB inverters. Among multilevel modulation techniques, carrier-based SPWM methods dominate industrial applications due to their adaptability and low cost. Phase Disposition (PD-PWM) and Phase Shift (PS-PWM) are two typical implementations. This section compares these methods using a three-cascaded H-bridge topology.

As shown in Figure 2, a three-cascaded system requires six carrier signals synchronized with the reference signal $Vref = 3mE\ sin(\omega mt)$, where m and ω_m represent the modulation ratio and angular frequency, respectively. In PD-PWM, carriers are vertically stacked with synchronized phases and amplitude intervals of E. In PS-PWM, carriers are horizontally staggered with a 60° phase shift. These configurations generate distinct switching sequences.

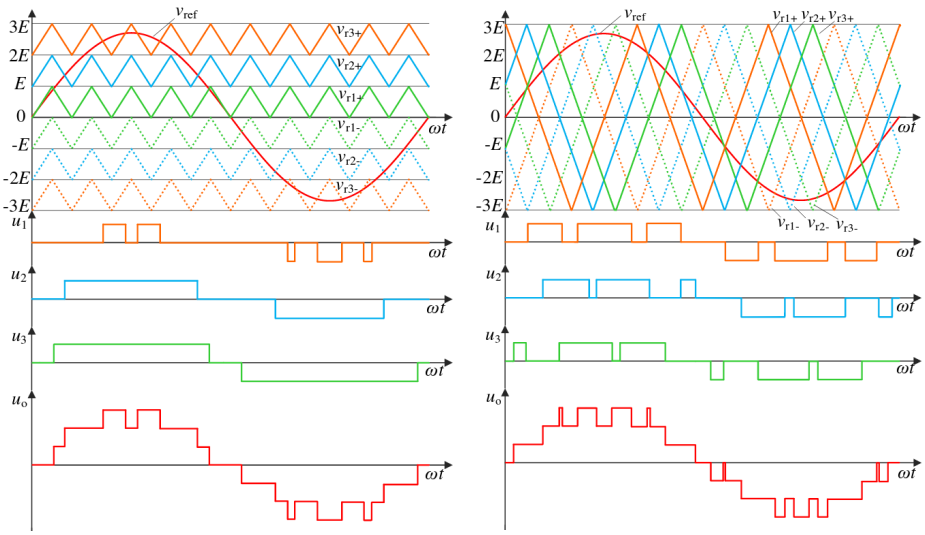


Figure 2. Modulation principles of two multi-carrier schemes.

Simulation waveforms in Figure 3 show that PD-PWM produces seven-level line voltages with continuous transitions, while PS-PWM increases levels to eleven but introduces discontinuous transitions due to overlapping carrier phases.

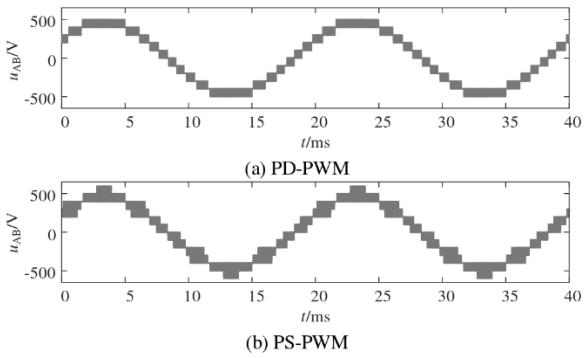


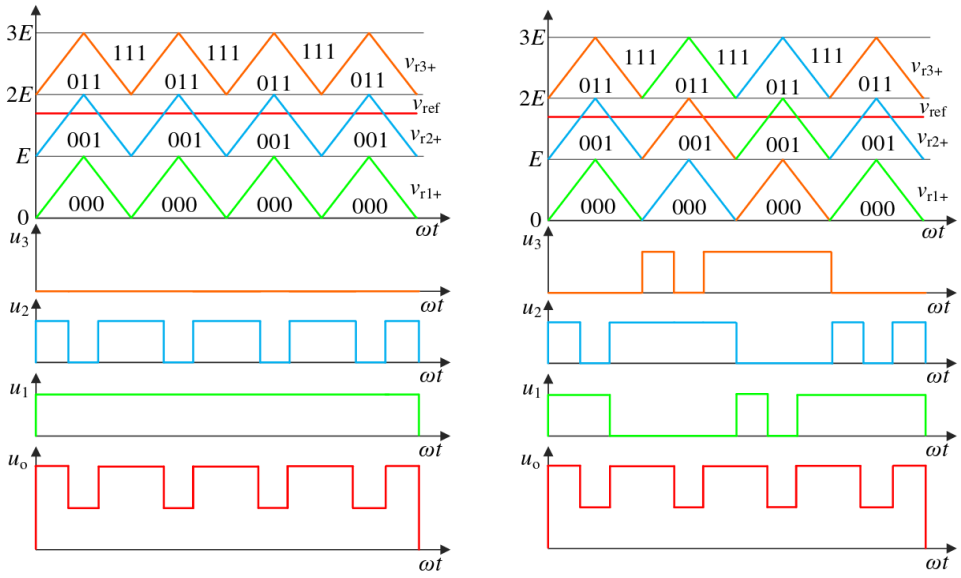
Figure 3. Line voltage waveforms under two modulation methods.

3. Optimized Modulation Strategy

While PD-PWM exhibits excellent harmonic suppression, its inherent carrier phase synchronization causes power imbalance among units. To address this, we propose a dynamic carrier reconstruction framework by decoupling carrier parameters (amplitude, phase, offset) to achieve power flow redistribution without compromising harmonic performance.

3.1. Carrier Degree-of-Freedom Control Concept

PD-PWM relies on sinusoidal reference waves interacting with vertically stacked carriers to generate switching signals. By reconstructing carrier parameters (e.g., vertical offsets) while fixing reference wave parameters, redundant switching states are introduced (Figure 4). This enables dynamic power redistribution while maintaining output stability.



(a) Pre-adjustment **(b) Post-adjustment.**

Figure 4. Relationship between output voltage and carrier degree of freedom.

3.2. Power Balancing via Carrier Cycle Rotation

Figure 5 illustrates the carrier phase rotation mechanism. Carrier clusters (vc1+/vc2+/vc3+ and vc1-/vc2-/vc3-) undergo periodic phase shifts within a $0.5T_0$ window, achieving spatiotemporal power balancing. Theoretical analysis shows an optimal balancing cycle of $1.5T_0$. The output waveform exhibits quarter-cycle symmetry, breaking traditional half-cycle symmetry.

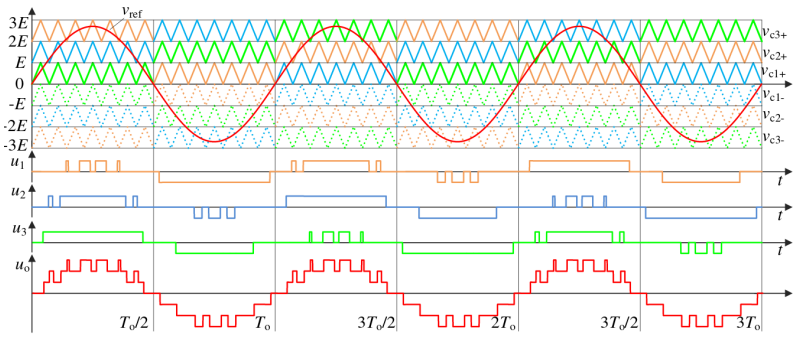
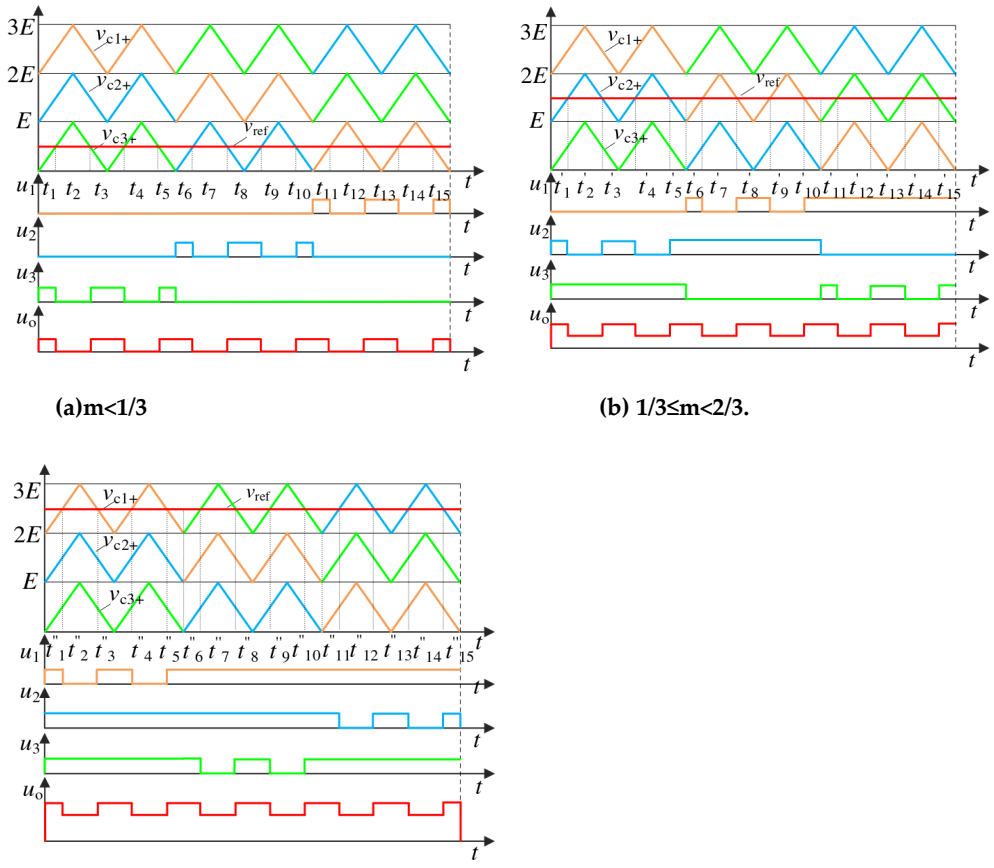


Figure 5. Carrier cycle rotation modulation strategy.

3.3. Power balancing scheme

Building upon the carrier vertical offset control method at the output cycle level described in Section 2.2, this section innovatively proposes a dynamic balancing modulation strategy at the carrier cycle level. By establishing an inter-layer migration mechanism for triangular carriers, the strategy constructs a periodic carrier cycling framework with the carrier period Tc as the fundamental time unit, forming a cycle duration of $2nT_c$ (where n denotes the total number of cascaded units). As illustrated in Figure 5, within a 6Tc time window, the carrier signals for the left and right bridge arms of each unit complete full migration cycles across layers 1–3 and layers 4–6, respectively. When the carrier frequency f_c significantly exceeds the modulation frequency fm (fc >> fm), the modulation wave amplitude can be approximated as maintaining quasi-static characteristics during a single cycling period Tr (Tr = 6Tc). The modulation index-level state mapping relationship depicted in Figure 6 reveals distinct patterns in the level-holding time parameter sets Tr = 6Tc, tx、t'x、t''x (x = 1,2,…,15) across cascaded units under varying modulation indices.



(a)m<1/3 **(b) 1/3≤m<2/3.**

(c) 2/3≤m≤1.

Figure 6. Output voltage under different modulation degrees.

4. Simulation and Experimental Analysis

A Simulink-based three-cascaded H-bridge inverter model was constructed for validation. The experimental data in Figure 7 reveal the power distribution characteristics of the novel modulation strategy under a wide range of modulation ratios. When the modulation ratio m varies within the range of 0.3–1.0, the instantaneous power curves of the three power units consistently exhibit highly synchronized waveform characteristics, with their period-averaged power ratios stabilized within the range of 0.99:1.00:1.01 (standard deviation < 2%). This phenomenon confirms that the proposed algorithm possesses adaptive balancing capability comparable to PS-PWM, while achieving approximately 40%

faster balancing response compared to traditional carrier rotation schemes (reducing the theoretical derivation from $1.5T_0$ to $0.9T_0$. Power transient analysis demonstrates that the system completes power rebalancing within 3 carrier cycles, with an error rate below 4.5% compared to numerical simulation results. These findings validate the significant advantages of the carrier dynamic recombination mechanism in rapid equilibrium control.

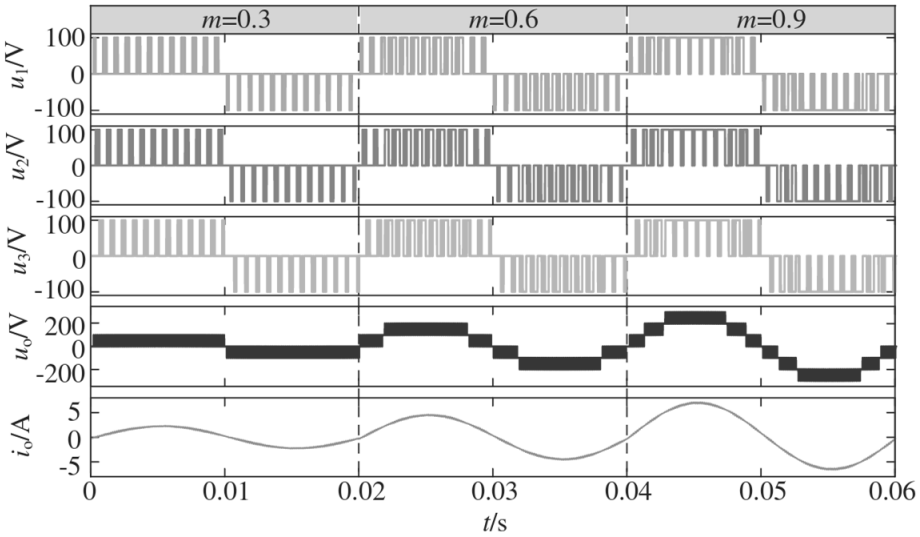


Figure 7. Simulation waveforms of inverter output under varying modulation indices.

Figure 8 demonstrates power distribution across the full modulation range m = 0.3–1.0. Instantaneous power curves remain synchronized, with average power ratios stabilized at 0.99:1.00:1.01 (standard deviation < 2%). The proposed strategy achieves 40% faster balancing than traditional carrier rotation ($1.5T_0$ to $0.9T_0$). Transient analysis shows power rebalancing within three carrier cycles, with <4.5% error relative to simulations.

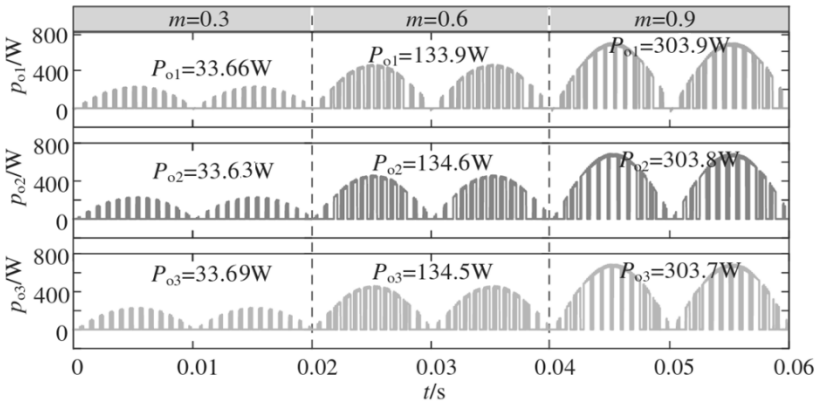


Figure 8. Power distribution under novel modulation strategy.

To complete the empirical research of the control strategy, a three-level cascaded H-bridge inverter hardware validation platform was constructed. The experimental system adopts a modular design architecture, with a real-time control system based on a TI F28335 digital signal processor (DSP). The power-stage parameter configuration includes: DC bus voltage of 25 V, resistive load of 24 Ω, filter inductance of 5.5 mH, load resistance R = 24Ω, and a carrier ratio design of 340:1 formed by a modulation wave frequency of 50 Hz and a carrier frequency of 17 kHz. (This parameter configuration fully considers the balance between switching losses of power devices and system dynamic response.)

The output power distribution of each cascaded unit obtained by the new modulation method is shown in Figure 9. By importing the power data from Figure 9 into

MATLAB, it can be observed that this modulation strategy maintains a power ratio of Po1:Po2:Po3 ≈ 1:1:1 under different modulation ratios. Therefore, this modulation method can achieve power balance control of each unit across various modulation ratios.

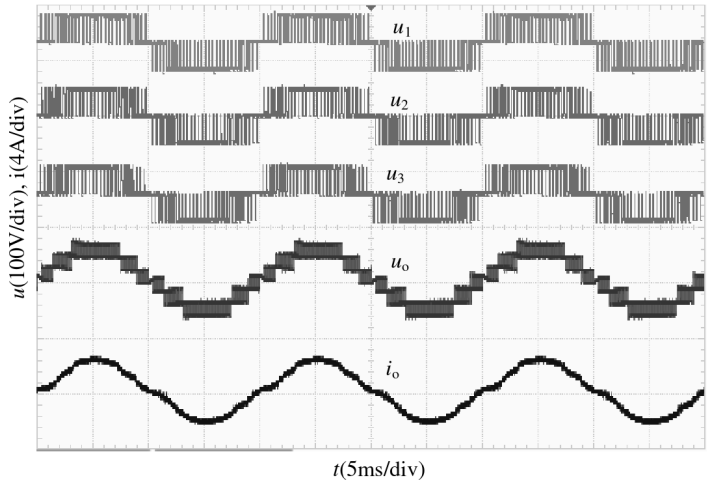


Figure 9. Experimental waveforms of the novel balancing modulation strategy.

5. Conclusion

This study systematically analyzes symmetric CHB inverter topologies and evaluates PD-PWM and PS-PWM modulation strategies. While PS-PWM inherently balances power, its discontinuous transitions weaken harmonic suppression. PD-PWM excels in harmonic suppression but suffers from power imbalance. The proposed dynamic carrier reconstruction framework overcomes these limitations through:

1. Vertical carrier offset control as an independent degree of freedom for power redistribution without altering macroscopic output.

2. Inherited harmonic suppression from PD-PWM, with experimentally verified THD reduction compared to PS-PWM.

3. Enhanced balancing speed, achieving 40% faster response than traditional carrier rotation.

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